

## DM74ALS874B

### Dual 4-Bit D-Type Edge-Triggered Flip-Flop with 3-STATE Outputs

#### General Description

This dual 4-bit register features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. It is particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the DM74ALS874B are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

#### Features

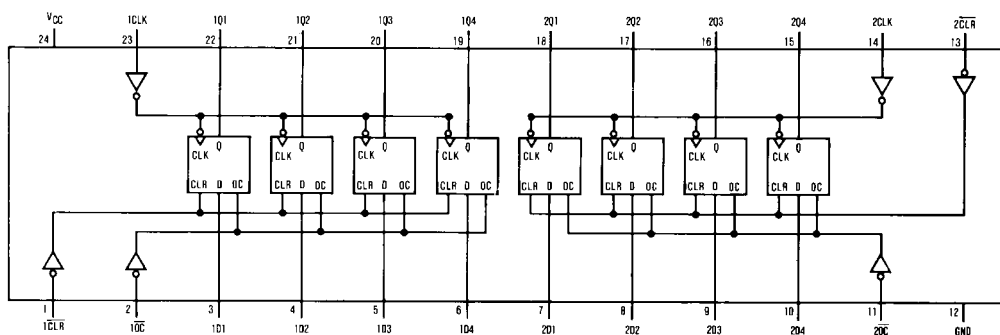
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and  $V_{CC}$  range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package
- Asynchronous clear

#### Ordering Code:

Order Number	Package Number	Package Description
DM74ALS874BWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74ALS874BNT	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram

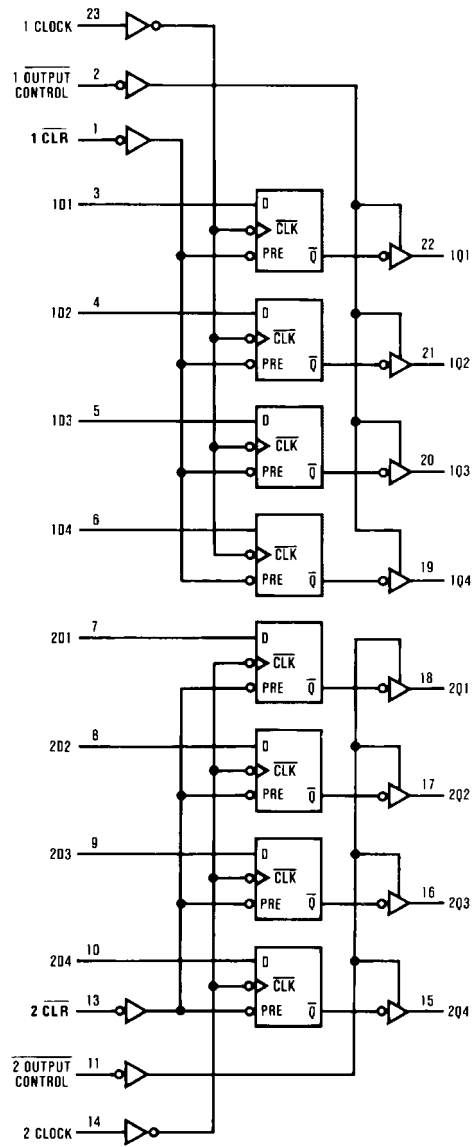


Function Table

Inputs				Output
CLR	D	CLK	OC	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q <sub>0</sub>

L = LOW State  
 H = HIGH State  
 X = Don't Care  
 ↑ = Positive Edge Transition  
 Z = High Impedance State  
 Q<sub>0</sub> = Previous Condition of Q

Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical $\theta_{JA}$	
N Package	51.0°C/W
M Package	86.5°C/W

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.5	5	5.5	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			-2.6	mA
$I_{OL}$	LOW Level Output Current			24	mA
$f_{CLK}$	Clock Frequency	0		30	MHz
$t_{WCLK}$	Width of Clock Pulse	HIGH	16.5		ns
		LOW	16.5		ns
$t_{WCLR}$	Width of Clear Pulse	LOW	10		ns
$t_{SU}$	Data Setup Time (Note 2)	15 $\uparrow$			ns
$t_H$	Data Hold Time (Note 2)	0 $\uparrow$			ns
$t_{SU}$	Clear Inactive	12			ns
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 2:** The ( $\uparrow$ ) arrow indicates the positive edge of the Clock is used for reference.

## Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

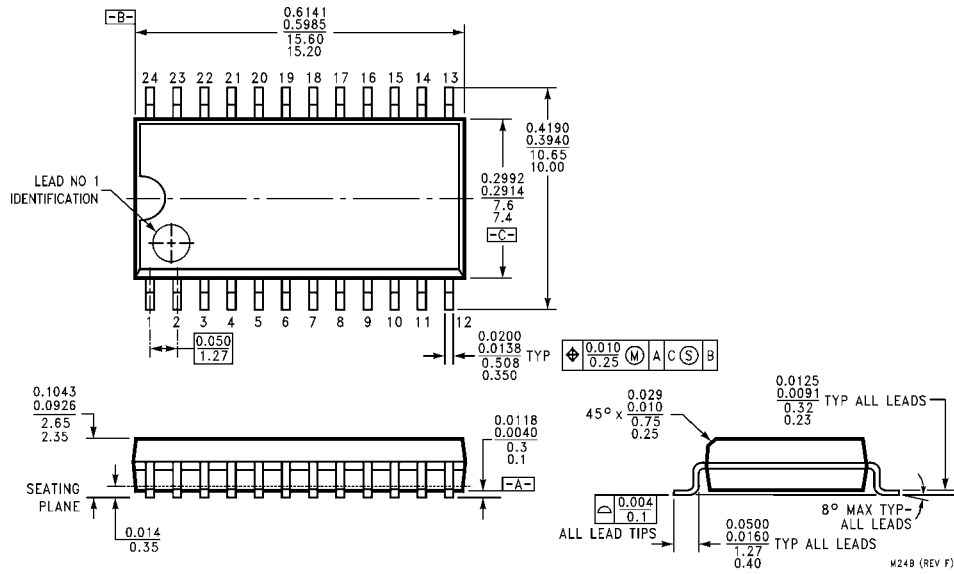
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$V_{IK}$	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_I = -18\text{ mA}$			-1.2	V	
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL\text{ Max}}$	$I_{OH} = \text{Max}$	2.4	3.2	V	
		$V_{CC} = 4.5V\text{ to }5.5V$	$I_{OH} = -400\ \mu A$	$V_{CC} - 2$		V	
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	$I_{OL} = 12\text{ mA}$		0.25	0.4	V
			$I_{OL} = 24\text{ mA}$		0.35	0.5	V
$I_I$	Input Current @ Maximum Input Voltage	$V_{CC} = 5.5V$ , $V_{IH} = 7V$			0.1	mA	
$I_{IH}$	HIGH Level Input Current	$V_{CC} = 5.5V$ , $V_{IH} = 2.7V$			20	$\mu A$	
$I_{IL}$	LOW Level Input Current	$V_{CC} = 5.5V$ , $V_{IL} = 0.4V$			-0.2	mA	
$I_O$	Output Drive Current	$V_{CC} = 5.5V$ , $V_O = 2.25V$	-30		-112	mA	
$I_{OZH}$	OFF-State Output Current HIGH Level Voltage Applied	$V_{CC} = 5.5V$ , $V_{IH} = 2V$			20	$\mu A$	
		$V_O = 2.7V$					
$I_{OZL}$	OFF-State Output Current LOW Level Voltage Applied	$V_{CC} = 5.5V$ , $V_{IH} = 2V$ $V_O = 0.4V$			-20	$\mu A$	
$I_{CC}$	Supply Current	$V_{CC} = 5.5V$ Outputs OPEN	Outputs HIGH		14	21	mA
			Outputs LOW		19	30	mA
			Outputs Disabled		20	32	mA

## Switching Characteristics

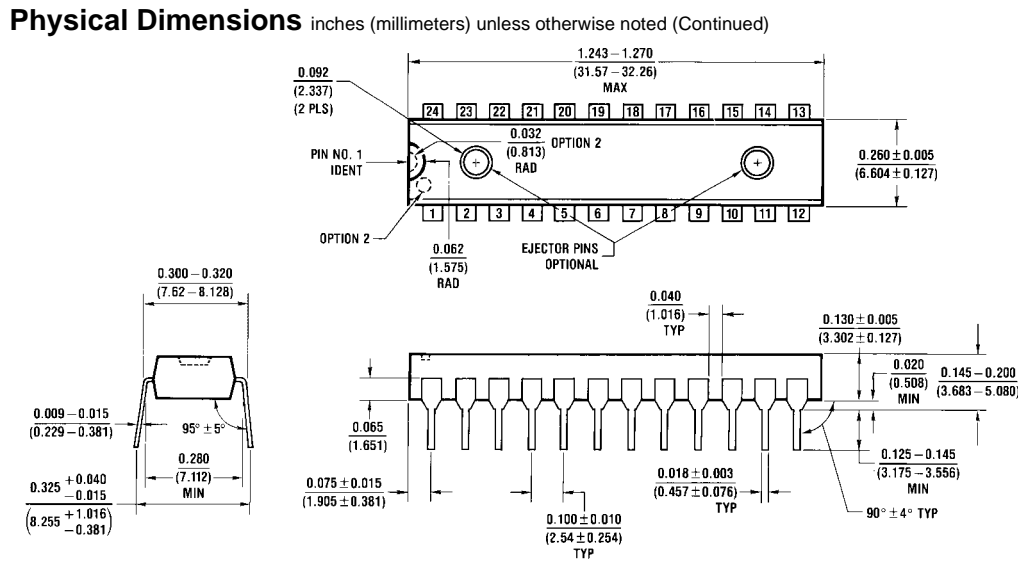
over recommended operating free air temperature range.

Symbol	Parameter	Conditions	From	To	Min	Max	Units
$f_{MAX}$	Maximum Clock Frequency	$V_{CC} = 4.5V\text{ to }5.5V$			30	MHz	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	$R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$	Clock	Any Q	4	14	ns
			Clock	Any Q	4	14	ns
Output Enable Time to HIGH Level Output	Output Control		Any Q	4	18	ns	
Output Enable Time to LOW Level Output	Output Control		Any Q	4	18	ns	
Output Disable Time from HIGH Level Output	Output Control		Any Q	2	10	ns	
Output Disable Time from LOW Level Output	Output Control		Any Q	3	12	ns	
Propagation Delay Time HIGH-to-LOW Level Output	Clear		Any Q	5	17	ns	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M24B**



N24C (REV F)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
 Package Number N24C**

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